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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,716	03/24/2004	Kalyan Muthukumar	42P18140	8094
8791	7590	02/05/2008		
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 1279 OAKMEAD PARKWAY SUNNYVALE, CA 94085-4040			EXAMINER VU, TUAN A	
			ART UNIT 2193	PAPER NUMBER
			MAIL DATE 02/05/2008	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication..

## Office Action Summary

Application No.

10/809,716

Applicant(s)

MUTHUKUMAR ET AL.

Examiner

Tuan A. Vu

Art Unit

2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-38 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>3/24/04</u> .   | 6) <input type="checkbox"/> Other: _____                          |

### DETAILED ACTION

1. This action is responsive to the application filed 3/24/2004.

Claims 1-38 have been submitted for examination.

#### *Claim Objections*

2. Claims 8 is objected to because of the following informalities: there appears to be an extraneous 'for' in 'adding an entry to the ready **for** list for any instruction'. Appropriate correction is required.

#### *Claim Rejections - 35 USC § 101*

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The Federal Circuit has recently applied the practical application test in determining whether the claimed subject matter is statutory under 35 U.S.C. § 101. The practical application test requires that a "useful, concrete, and tangible result" be accomplished. An "abstract idea" when practically applied is eligible for a patent. As a consequence, an invention, which is eligible for patenting under 35 U.S.C. § 101, is in the "useful arts" when it is a machine, manufacture, process or composition of matter, which produces a concrete, tangible, and useful result. The test for practical application is thus to determine whether the claimed invention produces a "useful, concrete and tangible result".

The current focus of the Patent Office in regard to statutory inventions under 35 U.S.C. § 101 for method claims and claims that recite a judicial exception (software) is that the claimed invention recite a practical application. Practical application can be provided by a physical transformation or a useful, concrete and tangible result. The following link on the World Wide Web is for the United States Patent And Trademark Office (USPTO) policy on 35 U.S.C. § 101.

[http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101\\_20051026.pdf](http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf)

4. Claims 25-31 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Specifically, claim 25 recites a compiler, a front end and a code generator, all of which perceived from the Disclosure as software implemented entities. The claim amounts to listing of

mere Functional Descriptive Material (see Annex IV of USC101 Guidelines, pg. 52-54); that is, absent hardware support to materialize functionality of listed code instructions, software per se cannot be construed as a permissible statutory category able to yield a real world result (i.e. concrete, tangible, and useful result provided by data transformation from Practical Application implementing one of the 4 statutory categories) via code execution by machine support. Claims 25-31 are rejected under 35 U.S.C. 101 because they are directed to non-statutory subject matter.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 5, 9-15, 17, 21-30, 32-38 are rejected under 35 U.S.C. § 102(b), as being anticipated by Kumar et al, USPN: 7,007,271 (hereinafter Kumar )

**As per claim 1**, Kumar discloses a method comprising: determining a slack value for each of one or more ready instructions based on resource constraints (slack value – col. 14, lines 4-31); selecting one of the ready instructions, based on the slack value (e.g. priority function - col. 14, lines 15-31); and scheduling the selected ready instruction (e.g. step 105—115, select instruction step 155 – Fig. 1).

**As per claim 2**, Kumar discloses performing the method set forth in claim 1 until all instructions in a scheduling region have been scheduled (e.g. Fig. 1).

**As per claim 3**, Kumar discloses determining a slack value (priority function - col. 14, lines 15-31; Fig. 1) for each of the one or more ready instructions further comprises determining the slack value for the instruction based on resource constraints and dependence height (e.g. *total number resources, maximum latency dependencies, larger of the dependencies or resource constraints, longest delay ... resource, latency*— col. 12, line 62 to col. 14, line 5).

**As per claim 5**, Kumar discloses selecting one of the ready instructions further comprises selecting a ready instruction having a lowest slack value (priority function 115, Fig. 1; *earliest scheduling time ... least number of slacks* – col. 14, lines 4-25).

**As per claims 9-10**, Kumar discloses determining a minimum number of cycles needed to schedule the instructions of a scheduling region, taking resource constraints into account (*earliest scheduling time ... least number of slacks* – col. 14, lines 4-25); wherein the minimum number of cycles is determined to be a dependence length of the scheduling region if the scheduling region is dependence-bound (e.g. *minimum number of cycles, dependence ... constraints* – col. 13, lines 56-63; FSA automata – col. 11 – Note: priority function based on incremental building of a state machine reads on being dependent of graph length per region); and the minimum number of cycles is determined to be a resource length of the scheduling region if the scheduling region is resource-bound (e.g. *minimum number of cycles ... resources constraints* - col.13, lines 56-63; graph coloring – Table 15 - Note: register coloring function based on incremental building of a state machine reads on being dependent of resource length of a region).

**As per claim 11**, Kumar discloses calculating the dependence length of the scheduling region based on the total height (e.g. graph D ... 7 edges – col 4, ines 41-45; Table 2, col. 4;

Table 4-5, col. 5 – Note: spanning a incremental graph to color regions based on register allocations reads on total height of such spanned regions being colored) of a dependence graph of the scheduling region; and calculating the resource length of the scheduling region based on the maximum number of cycles needed (e.g. R total number resources, maximum latency instruction class – col. 11, lines 45-53; col. 12, lines 62-64; col. 13, lines 3-6) to schedule the instructions of the scheduling region for a machine resource.

**As per claim 12**, Kumar discloses wherein: the resource constraints include the maximum number of instructions of a particular instruction type (e.g. MAX Latency 3 col. 13, lines 3-5; *longest path ... for scheduling, longest delay, longest scheduling time, number of possible slots an instruction can be scheduled* - col. 13 line 64 to col. 14, line 9) that can be scheduled during a given cycle for a selected target processor.

**As per claim 13**, Kumar discloses an article comprising: a storage medium having a plurality of machine accessible instructions, which if executed by a machine, cause the machine to perform the following operations:

determining a slack value for each of one or more ready instructions based on resource constraints;

selecting one of the ready instructions, based on the slack value; and

scheduling the selected ready instruction;

all of which operations having been addressed in claim 1.

**As per claims 14-15, 21-24**, refer to claims 2-3, 9-12, respectively.

**As per claim 17**, Kumar discloses that the selected ready instruction is having highest scheduling priority: since Kumar set forth an instruction for scheduling and updating this

scheduling (col. 13-14) by a heuristics operating on the result of a *priority function* (e.g. step 115 - Fig. 1), Kumar also discloses that priority is given to said instruction by virtue of the priority function computing.

**As per claim 25**, Kumar discloses compiler comprising:

a front end; and a code generator; wherein the code generator includes one or more resource-aware schedulers to schedule instructions, the one or more resource-aware schedulers to take resource constraints into account (e.g. incremental interference graph, graph coloring, finite state automata, Finite state table generation col. 6-13; Priority Update and Fig. 1 ) to generate a slack value (col. 14, lines 5-35) for each of the instructions (step 155, Fig 1).

**As per claim 26**, Kumar, in view of the rationale of claim 4 or 16, discloses that one or more resource-aware schedulers determines a first scheduling deadline for an instruction in a scheduling region, *taking dependence considerations into account*; and said one or more resource-aware schedulers is further to determine a second scheduling deadline for the instruction, *taking resource constraints into account*; and said one or more resource-aware schedulers is further to select between the first and second scheduling deadlines to choose a scheduling priority (i.e. a selected slack value) for the instruction.

**As per claim 27-28**, Kumar discloses wherein said resource-aware scheduler is further to select among ready instructions to select an instruction for scheduling (re claim 5); wherein said resource-aware scheduler is further to select the instruction for scheduling based on its scheduling priority (re claim 17).

**As per claim 29**, Kumar discloses the maximum number of *instructions (e.g. number of all possible ... an instruction can be scheduled* – col. 14, lines 3-11) that can be scheduled per cycle.

**As per claim 30**, refer to claim 12.

**As per claim 32**, Kumar discloses a system comprising: a processor; and a memory system to store instructions; wherein the instructions include a resource-aware scheduler to determine, based on resource constraints (refer to claim 25), a slack-based scheduling priority for each of one (refer to claim 25) or more instructions.

**As per claim 33**, Kumar discloses wherein: the memory system includes a DRAM (e.g. memory load instruction – col. 21, lines 8-9).

**As per claim 34**, refer to rationale as set forth in claim 26.

**As per claims 35-38**, refer to claims 27-30, respectively.

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A person shall be entitled to a patent unless –

(a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 4, 6-8, 16, 18-20, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar, further in view of Cooper et al, ‘An Experimental Evaluation of List Scheduling’, , Rice University, , pp. 1-15 (hereinafter Cooper) – September 1998, date as of



TR98-326 (refer to Technical Reports pg. 12, bottom, in provided Devika Subramanian, portfolio)

**As per claim 4**, Kumar determining a slack value further comprises: determining a dependence basis based on a dependence height for the instruction (refer to claim 11); determining a resource basis based on resource constraints for the instruction (refer to claim 10); selecting between the resource basis and the dependence basis to choose a slack value that indicates a least number of cycles (e.g. *longest path ... for scheduling, longest delay, longest scheduling time, number of possible slots an instruction can be scheduled* - col. 13 line 64 to col. 14, line 9); and determining the slack value based on the selected dependence/resource basis value (e.g. col. 13, line 63 to col. 15, line 25).

But Kumar does not explicitly teach that such dependence (i.e. tree region span) or resource basis (i.e. register analysis and region coloring) is respectively called *dependence* and *resource deadline*. However, slack calculation by Kumar entails either a maximum of latency, path size or slots to be scheduled per region spanned by a class of instruction (col. 14 line 8-31; re claim 10-11) based on resources or spanning of sub-region in term of size of edge dependencies ( see claim 11), hence the concept of end limit is integral to those tree size basis or register dependency basis. It would have been obvious for one skill in the art at the time the invention was made to implement a deadline value for each of said tree spanning analysis and register-based coloring basis by Kumar so that a slack value can be based on selecting between either a dependence deadline or a resource deadline, in view of Kumar's optimizing a value based on path spanning and delay analysis as set forth in the priority function heuristics as set forth for this slack value deriving ( e.g. Fig. 1; col. 14 lines 4-31)

As per claims 6, 8, Kumar teaches heuristics to build into a state graph per advance of cycle and evaluate metrics per graph node upon each edge transition (see col. 11; Fig. 1) but does not explicitly disclose generating an entry in a ready list for each of the one or more ready instructions; and removing the entry for the selected ready instruction from the ready list; nor does Kumar disclose advancing a virtual clock to a subsequent clock cycle; and adding an entry to the ready for list for any instruction that becomes ready in the subsequent clock cycle.

Analogous to a graph heuristics building by Kumar, Cooper also teaches computing metrics related to minimum schedule length in the context of evaluation critical path (sec 5, pg. 7-9) similar to Kumar's priority function (Kumar: heuristics ... critical path – col. 13-14); and further provides computation of priority function (sec 3-4, pg. 3-4 – which is analogous to Kumar's Fig. 1) related to graph depth and cycle latency heuristics with a algorithm, and according to which algorithm Cooper teaches a per-time-cycle (clock cycle ) *ready list* of DPG nodes and remove nodes therefrom (see *ready-list, time cycle* - Algorithm pg. 4) in the course of calculating their respective priorities (Input, Output Data Precedence Graph – pg. 4, top). It would have been obvious for one skill in the art at the time the invention was made to implement the heuristics by Kumar so that each instruction identified from a dependence graph per cycle analysis (Kumar: Fig. 1) would be inputted into a ready list as by Cooper for calculating constraints metrics therefor per cycle clock advance, including removing the 'ready' instruction from said list once this evaluation is done; because this is how Kumar intends to find the optimum value for each and every instructions pertinent to a region of dependency tree, as evidenced by Cooper, such that a 'ready' list is created and depleted in function of the traversal of node in said tree by the algorithm.

**As per claim 7**, Kumar does not explicitly disclose adding to an uncover list any instructions uncovered by the scheduling of the selected ready instruction. But Cooper teaches a heuristics by which an covering of a instruction from a ready-list a instruction is identified (or uncovered) as being entered in another list from an evaluation covered under some predicate (Cooper: *if (a functional unit ... and add to the inflight-list* – Algorithm pg. 4). One would be motivated to implement Cooper's uncover list to Kumar's heuristics to better segregate ready list as set forth above from a uncover list, and thereby keeping track of the amount of instructions per clock already covered from executing Kumar's priority calculation algorithm, based on the rationale as set forth in claim 6.

**As per claim 16**, refer to claim 4.

**As per claims 18, 20**, refer to the rationale of claims 6, 8.

**As per claim 19**, refer to claim 7.

**As per claim 31**, Kumar does not explicitly disclose wherein: the resource-aware scheduler is further to schedule the instructions such that instructions of a particular instruction type are distributed evenly among two or more resources. But based on the resources analysis and the dependencies of tree spanning and finite state recording by Kumar ( see incremental interference graph, graph coloring, finite state automata, Finite state table generation col. 6-13;) leading to *priority function* computing to update the number of registers (see steps 175, 180 – Fig. 1) for a best slack value (col. 14, lines 5-35), it would have been obvious for one skill in the art at the time the invention was made to implement the above register update so that based on the slack value approach, Kumar reschedules a type of instruction (see step 155, Fig. 1) so that it is evenly distributed among the available registers, because of all of which would be more

feasible as a result of the role played in Kumar's front end creation of incremental dependence graph and finite state building coupled to graph coloring as set forth above.

*Conclusion*

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (571) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 ( for non-official correspondence - please consult Examiner before using) or 571-273-8300 ( for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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February 04, 2008

2-4-08

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